LogiCORE IP Clocking Wizard v3.1

DS709 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP Clocking Wizard core makes it easy to create HDL source code wrappers for clock circuits customized to your clocking requirements. You can either let the wizard select an appropriate clocking primitive for you automatically, then configure buffering, feedback, and timing parameters for your desired clocking network, or you can manually select the primitive and configure all aspects of the primitive and clocking network yourself. The wizard guides you in the setting of the appropriate attributes for your clocking primitive, and at the same time also allows you to override any wizard-calculated parameter.

Besides providing an HDL wrapper to implement the desired clocking circuit, the Clocking Wizard also delivers a timing parameter summary generated by the Xilinx timing tools for the circuit.

Features

- Accepts up to two input clocks and up to seven output clocks per clock network
- Automatically chooses correct clocking primitive for a selected device
- Automatically configures clocking primitive based on user-selected clocking features
- Automatically calculates Voltage Controlled Oscillator (VCO) frequency for primitives with an oscillator, and provides multiply and divide values based on input and output frequency requirements
- Automatically implements overall configuration that supports phase shift and duty cycle requirements
- Provides the ability to override the selected clock primitive and any calculated attribute
- Optionally buffers clock signals
- Provides timing estimates for the clock circuit and Xilinx® Power Estimator (XPE) parameters
- Provides a synthesizeable example design including the clocking network and a simulation test bench
- Provides optional ports for the selected primitive

LogiCORE IP Facts				
Core Specifics				
Supported Device Family (1)	Virtex-7 Virtex-6 Spartan-6 Kintex-7			
Supported User Interfaces	Not Applicable			
Resources Used	I/O	LUTs	FFs	Block RAMs
	1-2	0-1	0	0
Special Features	DCM, DCM_CLKGEN, MMCM, PLL, MMCME2			
Provided with Core				
Documentation	Product Specification Getting Started Guide Release Notes			
Design Files	Verilog and VHDL			
Example Design	Verilog and VHDL			
Test Bench	Verilog and VHDL			
Constraints File	.ucf (user constraints file)			
Simulation Model	UniSim			
Instantiation Template	Verilog and VHDL Wrapper			
Additional Items	7 Series FPGAs Clocking Resources User Guide Virtex-6 and Spartan-6 User Guides			
Tested Design Tools				
Design Entry Tools	ISE v13.1 software			
Simulation	Mentor Graphics ModelSim v6.6d, Cadence Incisive Enterprise Simulator (IES) v10.2, Synopsys VCS and VCS MX 2010.06, ISIM			
Synthesis Tools	Synplify PRO E-2011.03, XST			
Support				
Provided by Xilinx, Inc.				

1. For the complete list of supported devices, see the release notes for this core.

Functional Overview

The Clocking Wizard is an interactive Graphical User Interface (GUI) that creates a clocking network based on design-specific needs. The required clock network parameters are organized in a linear sequence so that you can select only the desired parameters. Using the wizard, experienced users can explicitly configure their chosen clocking primitive, while less experienced users can let the wizard automatically determine the optimal primitive and configuration -- based on the features required for their individual clocking networks.

Users already familiar with the Digital Clock Manager (DCM) and Phase-Locked Loop (PLL) wizards may refer to the Migration Guide Appendix in the Clocking Wizard Getting Started Guide for information on usage differences.

Clocking Features

Major clocking-related functional features desired and specified by the user can be used by the wizard to select an appropriate primitive. Incompatible features are automatically dimmed out to help the designer evaluate feature trade-offs.

Clocking features include:

- Frequency synthesis
- Phase alignment
- Minimization of output jitter
- Allowance of larger input jitter
- Minimization of power
- Dynamic phase shift
- Dynamic reconfiguration

Input Clocks

One input clock is the default behavior, but two input clocks can be chosen by selecting a secondary clock source. Only the timing parameters of the input clocks in their specified units is required; the wizard uses these parameters as needed to configure the output clocks.

Note: For Spartan®-6 FPGA designs, the ISE® tool chain infers BUFIO2 for input clock routing which is not part of the generated HDL.

Input Clock Jitter Option

The wizard allows the user to specify the input clock jitter either in UI or PS units using a radio button.

Output Clocks

The number of output clocks is user-configurable. The maximum number allowed depends upon the selected device and the interaction of the major clocking features you specify. Users can simply input their desired timing parameters (frequency, phase, and duty cycle) and let the clocking wizard select and configure the clocking primitive and network automatically to comply with the requested characteristics. If it is not possible to comply exactly with the requested parameter settings due to the number of available input clocks, best-attempt settings are provided. When this is the case, the clocks are ordered so that CLK_OUT1 is the highest-priority clock and is most likely to comply with the requested timing parameters. The wizard prompts you for frequency parameter settings before the phase and duty cycle settings. (Note that the port names in the generated circuit may differ from the port names used on the original primitive.)

Clock Buffering and Feedback

In addition to configuring the clocking primitive within the device, the wizard also assists with constructing the clocking network. Buffering options are provided for both input and output clocks. If a clock output requires special buffers like BUFPLL which the wizard does not generate in the design, alert messages are flagged to the user. Feedback for the primitive can be user-controlled or left to the wizard to automatically connect. If automatic feedback is selected, the feedback path is matched to timing for `CLK_OUT1`.

Optional Ports

All primitive ports are available for user-configuration. You can expose any of the ports on the clocking primitive, and these are provided as well in the source code.

Optional Attributes

The BUFR_DIVIDE attribute of BUFR is available for the user as a generic parameter in the HDL when the output driver is chosen as BUFR. The user can change the divide value of the BUFR while instantiating the design.

Primitive Override

All configuration parameters are also user-configurable. In addition, should a provided value be undesirable, any of the calculated parameters can be overridden with the desired settings.

Summary

The Clocking Wizard provides a summary for the created network. Input and output clock settings are provided both visually and as constraint files. In addition, jitter numbers for the created network are provided along with a resource estimate. Lastly, the wizard provides the input setting for PLL and MMCM based designs for Xilinx Power Estimator (XPE) in an easy-to-use table.

Design Environment

Figure 1 shows the design environment provided by the wizard to assist in integrating the generated clocking network into a design. The wizard provides a synthesizable and downloadable example design to demonstrate how to use the network and allows you to place a very simple clocking network in your device. A sample simulation test bench, which simulates the example design and illustrates output clock waveforms with respect to input clock waveforms, is also provided.

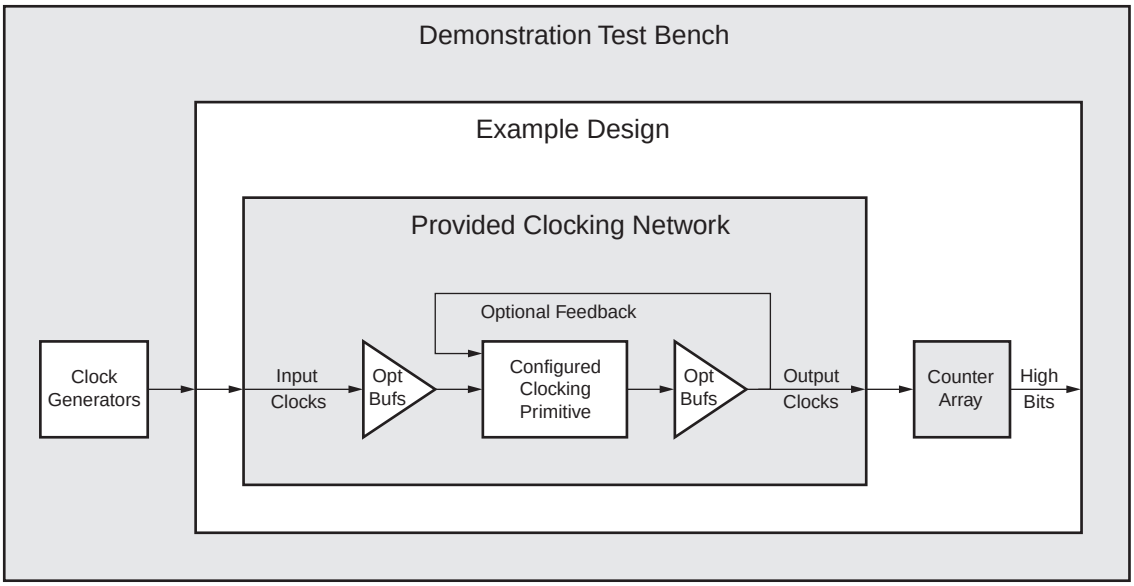

Figure 1: **Clocking Network and Support Modules Provided to the User**

I/O Signals

Table 1 describes the input and output ports provided from the clocking network. All ports are optional, with the exception being that at least one input and one output clock are required. The options selected by the user determine which ports are actually available to be configured. For example, when Dynamic Reconfiguration is selected, these ports are exposed to the user. Any port that is not exposed is appropriately tied off or connected to a signal labeled *unused* in the delivered source code. Not all ports are available for all devices or primitives; for example, Dynamic Reconfiguration is a feature only available in Virtex®-6 FPGA Mixed-Mode Clock Manager (MMCM), Spartan-6 FPGA DCM_CLKGEN, and Virtex-7 and Kintex™-7 FPGAs MMCME2 primitives.

Table 1: **Clocking Wizard IO**

Port (10)	I/O	Description
Input Clock Ports (1)		
CLK_IN1	Input	**Clock in 1**: Single-ended primary input clock port. Available when single-ended primary clock source is selected.
CLK_IN1_P	Input	**Clock in 1 Positive and Negative**: Differential primary input clock port pair. Available when a differential primary clock source is selected.
CLK_IN1_N		
CLK_IN2	Input	**Clock in 2:** Single-ended secondary input clock port. Available when a single-ended secondary clock source is selected.
CLK_IN2_P	Input	**Clock in 2 Positive and Negative:** Differential secondary input clock port pair. Available when a differential secondary clock source is selected.
CLK_IN2_N		
CLK_IN_SEL	Input	**Clock in Select:** When '1', selects the primary input clock; When '0', the secondary input clock is selected. Available when two input clocks are specified.
CLKFB_IN	Input	**Clock Feedback in**: Single-ended feedback in port of the clocking primitive. Available when user-controlled on-chip, user controller-off chip, or automatic control off-chip feedback option is selected.
CLKFB_IN_P	Input	**Clock Feedback in: Positive and Negative:** Differential feedback in port of the clocking primitive. Available when the automatic control off-chip feedback and differential feedback option is selected.
CLKFB_IN_N	Input	
Output Clock Ports		
CLK_OUT1	Output	**Clock Out 1:** Output clock of the clocking network. CLK_OUT1 is not optional.
CLK_OUT1_CE	Input	**Clock Enable:** Chip enable pin of the output buffer. Available when BUFGCE or BUFHCE or BUFR buffers are used as output clock drivers.
CLK_OUT1_CLR	Input	**Counter reset for divided clock output:** Available when BUFR buffer is used as output clock driver.
CLK_OUT2-n	Output	**Clock Out 2 - n:** Optional output clocks of the clocking network that are user-specified. For an MMCM, up to seven are available. For a PLL or DCM, up to six are available. For a DCM_CLKGEN, up to three are available.
CLK_OUT[2-n]_CE	Input	**Clock Enable:** Chip enable pin of the output buffer. Available when BUFGCE or BUFHCE or BUFR buffers are used as output clock drivers.
CLK_OUT[2-n]_CLR	Input	**Counter reset for divided clock output:** Available when BUFR buffer is used as output clock driver.
CLKFB_OUT	Output	**Clock Feedback Out:** Single ended feedback port of the clocking primitive. Available when the user-controlled feedback or automatic control off chip with single ended feedback option is selected.

Table 1: **Clocking Wizard IO *(Cont'd)***

Port [10]	I/O	Description
CLKFB_OUT_P	Output	**Clock Feedback Out: Positive and Negative:** Differential feedback output port of the clocking primitive. Available when the user-controlled off-chip feedback and differential feedback option is selected.
CLKFB_OUT_N	Output	
Dynamic Reconfiguration Ports for MMCM / MMCME2		
DADDR[6:0]	Input	**Dynamic Reconfiguration Address:** Address port for use in dynamic reconfiguration; active when DEN is asserted
DCLK	Input	**Dynamic Reconfiguration Clock:** Clock port for use in dynamic reconfiguration
DEN	Input	**Dynamic Reconfiguration Enable:** Starts a dynamic reconfiguration transaction
DI[15:0]	Input	**Dynamic Reconfiguration Data in:** Input data for a dynamic reconfiguration write transaction; active when DEN is asserted
DO[15:0]	Output	**Dynamic Reconfiguration Data Out:** Output data for a dynamic reconfiguration read transaction; active when DRDY is asserted
DRDY	Output	**Dynamic Reconfiguration Ready:** Completes a dynamic reconfiguration transaction
DWE	Input	**Dynamic Reconfiguration Write Enable:** When asserted, indicates that the dynamic reconfiguration transaction is a write; active when DEN is asserted
Dynamic Reconfiguration Ports for DCM_CLKGEN [2]		
PROGCLK	Input	**Program Clock**: Clock port for use in dynamic reconfiguration
PROGEN	Input	**Program Enable**: Starts a dynamic reconfiguration transaction
PROGDATA	Input	**Program Data**: Serial data stream to reprogram primitive settings
PROGDONE	Output	**Program Done**: When asserted, indicates that the reconfiguration transaction is complete
Dynamic Phase Shift Ports [3]		
PSCLK	Input	**Dynamic Phase Shift Clock:** Clock for use in dynamic phase shifting
PSEN	Input	**Dynamic Phase Shift Enable:** Starts a dynamic phase shift transaction
PSINCDEC	Input	**Dynamic Phase Shift increment/decrement:** When '1'; increments the phase shift of the output clock, when '0', decrements the phase shift
PSDONE	Output	**Dynamic Phase Shift Done:** Completes a dynamic phase shift transaction
Status and Control Ports [4]		
RESET	Input	**Reset:** When asserted, asynchronously clears the internal state of the primitive, and causes the primitive to re-initiate the locking sequence when released
POWER_DOWN [5]	Input	**Power Down:** When asserted, places the clocking primitive into low power state, which stops the output clocks
STATUS[2:0] [6]	Output	**Status:** Contains information about the state of the primitive. See the user guide for specific bit descriptions
FREEZE [7]	Input	**Freeze**: When asserted, prevents tap adjustment in the event that the input clock is lost
INPUT_CLK_STOPPED [8]	Output	**Input Clock Stopped:** When asserted, indicates that the selected input clock is no longer toggling
LOCKED	Output	**Locked:** When asserted, indicates that the output clocks are stable and usable by downstream circuitry

Table 1: **Clocking Wizard IO *(Cont'd)***

Port [10]	I/O	Description
CLK_VALID [9]	Output	**Clock Output Valid:** The CLK_VALID output is a logical combination of the DCM status ports which give the best indication that the input clock has been locked to, the DCM is functioning properly, and the output clocks are valid. When asserted, indicates the output clocks are valid.

Notes:

1. At least one input clock is required; any design has at least a CLK_IN1 or a CLK_IN1_P/CLK_IN1_N port. A secondary input clock is supported for Virtex-6 FPGAs only.
2. Dynamic reconfiguration ports are available for Virtex-6 FPGA MMCM or Spartan-6 FPGA DCM_CLKGEN primitives.
3. Dynamic phase shift ports are available for Virtex-6 FPGA MMCM or Spartan-6 FPGA DCM primitives.
4. Exposure of every status and control port is individually selectable.
5. The power-down port is available for the Virtex-6 FPGA MMCM primitive.
6. The status port is available for the Spartan-6 FPGA DCM and DCM_CLKGEN primitives.
7. The freeze port is available for the Spartan-6 FPGA DCM_CLKGEN primitive.
8. The input clock stopped port is available for the Virtex-6 FPGA MMCM and Spartan-6 FPGA DCM and DCM_CLKGEN primitives.
9. clk_valid port is available for DCM and DCM_CLKGEN.
10. This version of clocking wizard supports naming of ports as per requirements. The list mentioned in Table 1 is the default port list.

Table 2: **Optional Attributes in HDL**

Attribute	Description
CLK_OUT[1-7]_BUFR_DIV	The BUFR_DIVIDE attribute of clock outputs which have BUFR as output drivers.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The LogiCORE IP Clocking Wizard core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated using the Xilinx ISE CORE Generator™ software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v13.1.

For more information, visit the Clocking Wizard product web page. Information about additional Xilinx LogiCORE IP modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE IP modules and software, contact your local Xilinx sales representative.

List of Acronyms

Acronym	Spelled Out
DCM	Digital Clock Manager
FF	Flip-Flop
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HDL	Hardware Description Language
IES	Incisive Enterprise Simulator
IP	Intellectual Property
ISE	Integrated Software Environment
ISIM	ISE Simulator
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
PLL	Phase-Locked Loop
RAM	Random Access Memory
VCO	Voltage Controlled Oscillator
VCS	Verilog Compiled Simulator (Synopsys)
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
XPE	Xilinx Power Estimator
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
12/17/08	1.1.1	Xilinx Confidential DRAFT. Approved for external release under NDA only.
04/24/09	1.1	Initial major release. Supports core version 1.1 and Xilinx tools 11.1. Supports Spartan-6 and Virtex-6 devices.
06/24/09	1.2	Updated to support core version 1.2 and Xilinx tools 11.2.
09/16/09	1.3	Updated to support core version 1.3 and Xilinx tools 11.3.
12/02/09	1.4	Updated to support core version 1.4 and Xilinx tools 11.4.
04/19/10	1.5	Updated to support core version 1.5 and Xilinx tools 12.1.
07/23/10	1.6	Updated to support core version 1.6 and Xilinx tools 12.2.
09/21/10	1.7	Updated to support core version 1.7 and Xilinx tools 12.3.
12/14/10	1.8	Updated to support core version 1.8 and Xilinx tools 12.4.
03/01/11	3.1	Updated to support core version 3.1and Xilinx tools 13.1.

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